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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MITCHELL, JAMES M	
ART UNIT	PAPER NUMBER
2813	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/605,408	RIM, KERN	
	Examiner	Art Unit	
	James M. Mitchell	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to applicant's amendment filed December 12, 2006.

Declaration

The 1.131 declarations filed on April 21, 2006 under 37 CFR 1.131 has been considered but is ineffective to establish priority before February 7, 2002.

In order to establish actual reduction to practice proof is needed. M.P.E.P 715.07. General statements in broad terms about what the exhibits describe along with a general assertion that the exhibits describe a reduction to practice "amounts essentially to mere pleading, unsupported by proof or a showing of facts" and, thus, does not satisfy the requirements of 37 CFR 1.131(b).

The evidence submitted is insufficient to establish actual reduction to practice. Pursuant to M.P.E.P. 2138.05[R-5] besides the fact that there is no evidence that the complete process was done prior to the date alleged[1] there is no evidence to establish testing of SOI without the staining layer to insure that the strain remained. Moreover, even if the process was fully disclosed, "it is not enough to show that a method was performed...invention is not reduced to practice until it is established that the product made by the process is satisfactory." Because the invention is not a simple one, evidence of testing the product is required. *c.f* In re Ashai Americal Inc., 37 USPQ2d 1204, 1206 (Fed. Cir. 1995). In regards to testing, applicant merely asserts that it was done he "believe by deep UV Raman spectroscopy," without proof; this is mere

[1] E-mails arguably only suggest a step prior to removal of the strain layer.

pleading. While Chan's declaration purports to show results verification for strained silicon, the only strain shown is with SiGe [Attachment Page 3]. There is no proof of Si maintaining strain once attached to the insulation layer and after the straining layer was removed prior to February 7, 2002 as alleged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Currie (U.S. 2006/0014366).

Currie (Fig. 2A-8A) disclose:

(cl. 1, 13) A method of forming a strained silicon-on-insulator structure, the method comprising the steps of: forming a silicon layer (118; Par. 0051) on a strain-inducing layer ("SiGe"; Par. 0047)[2] so as to form a multilayer structure (Fig. 2A), the strain-inducing layer having a different lattice constant than silicon so that the silicon layer is strained during the forming step ("epitaxial growth"; Par. 0050) as a result of a lattice mismatch with the strain-inducing layer, and then bonding the multilayer structure to a substrate (154, Fig. 4) the bonding step being chosen from the group consisting of

[2] Same material as claimed

directly bonding a first insulating on (Par. 0059) and contacting the strained layer silicon layer of the multilayer substrate to a second insulating layer (152) on the substrate (154), the strained silicon layer (118) directly contacting the insulating region (152); and then removing the strain-inducing layer (Fig. 4-6; Par. 0062) to expose a surface of the strained silicon layer and to yield a strained silicon-on-insulator structure (Fig. 6) comprising the substrate (154), the insulating region (152), and the strained silicon layer (118) on the insulating region;

(cl. 2, 9) wherein the substrate is formed of a semiconductor material (Par. 0059);

(cl. 3, 23) wherein the strain-inducing layer is formed of a SiGe alloy, and the strained silicon layer is under tensile strain (CLAIM 21 of Currie; see also footnote 2);

(cl. 4) wherein the strained silicon layer (118) is formed by epitaxial growth on the strain-inducing layer (Par. 0050);

(cl. 5, 10, 14) the strain inducing layer is SiGe alloy (e.g. metal-semiconductor; Par. 0047) wherein the removing step comprises preferentially etching the strain-inducing layer with hydrofluoric acid (Par. 0062);

(cl. 6, 15) wherein the bonding step comprises directly bonding the first insulating layer on the strained silicon layer of the multilayer substrate to the second insulating layer on the substrate (Par.0059);

(cl. 7, 16) the bonding step comprises directly bonding the insulating layer on and contacting the strained silicon layer of the multilayer substrate to the semiconductor layer of the substrate (Par. 0062);

(cl. 8, 17) wherein the bonding step comprises directly bonding the first semiconductor layer of the substrate to the second semiconductor layer (Par. 0057) of the multilayer substrate and separated from the strained silicon layer by the insulating layer (152);

(cl. 11, cont. cl. 13) further comprising the step of forming an IC device (Fig. 8A), in the surface of the strained silicon laver;

(cl. 12, 19) the step of forming the IC device , comprises the steps of forming source and drain regions (214,216), in the surface of the strained silicon layer (118) so that the strained silicon layer defines a channel between the source region, and the drain region, the channel being in direct contact with the insulating layer (152);

(cl. 18) the removing step comprises one or more techniques chosen from the group consisting of wafer cleaving (Par. 0064);

(cl. 20) forming a gate electrode (212) separated from channel by insulating region (210);

(cl. 21) forming a gate oxide (210) on the surface of the strained silicon layer, and forming gate (212) on the oxide.

(cl. 22) using the semiconductor layer (Par. 0072) to form a first gate electrode separated from the channel by the insulating region; forming a gate oxide (e.g. 210) on the surface of the strained silicon layer (118) and ; forming a second gate electrode on the gate oxide (Fig. 20).

Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Yeo et al. (U.S. 2005/0003599).

Yeo (Fig 3, 4, 6) discloses (cl. 1, 13) a method of forming a strained silicon-on-insulator structure, the method comprising the steps of: forming a silicon layer (3) on a strain-inducing layer (2) so as to form a multilayer structure, the strain- inducing layer having a different lattice constant than silicon (Par. 0013) so that the silicon layer is strained as a result of a lattice mismatch with the strain-inducing layer, [also 5, 6, 8, 14,15,16] bonding [1] the multilayer structure to a substrate (4) so that an insulating layer (5) is between the strained silicon layer (3) and the substrate (4) [also 6] with the insulating layer comprising a first portion/ layer/ surface, top, on the substrate and a second layer, bottom, on the strained silicon layer directly contacting the insulating layer, and then removing the strain-inducing layer (500; Abstract) to expose a surface of the strained silicon layer (3) and to yield a strained silicon-on-insulator structure comprising the substrate (4), the insulating layer (5) on the substrate and the strained silicon layer (3) on the insulating layer; (cl. 2, 9) wherein the substrate is formed of a semiconductor material (Par 0016); (cl. 3, 4) and the inducing layer being SiGe and formed by expataxial growth (Par. 0013); (Cl. 10, 18) and the removing step comprises cleaving (Abstract); (Cl. 11) further forming an IC device (Fig 6); (cl. 12, 19) wherein the steps of forming an IC comprise the steps of forming source drain I strain material (Par. 0010, 00018) with a channel between (i.e. "MOSFET"); (cl. 17) and bonding a first semiconductor substrate (1) to a second semiconductor (4) of the multi layer; (cl. 20,

21) with a gate (7) separated from channel by the insulating material (5)and oxide (Par. 00148).

Claims 1, 6 and 13-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Cohen et al. (U.S. 2004/014254).

Cohen (Fig 6, 7) discloses (cl. 1, 13) a method of forming a strained silicon-on-insulator structure, the method comprising the steps of: forming a silicon layer (600) on a strain-inducing layer (520) so as to form a multilayer structure, the strain- inducing layer having a different lattice constant than silicon ("SiGe") so that the silicon layer is strained as a result of a lattice mismatch with the strain-inducing layer, [also 5, 6, 8, 14,15,16] bonding [1] the multilayer structure to a substrate (160) so that an insulating layer (150) is between the strained silicon layer (600) and the substrate (160) [also 6] with the insulating layer comprising a first portion/ layer/ surface, top, on the substrate and a second layer, bottom, on the strained silicon layer directly contacting the insulating layer, and then removing the strain-inducing layer (Fig 7) to expose a surface of the strained silicon layer (600) and to yield a strained silicon-on-insulator structure comprising the substrate (160), the insulating layer (150) on the substrate and the strained silicon layer (600) on the insulating layer;

Claim Rejections - 35 USC § 103

[1] Because the claim does not claim a particular order, bonding the insulating layer to the substrate can occur at any phase (i.e. prior/ after) contacting insulating layer to either a single silicon layer or combination silicon, strain inducing layer.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al. (U.S. 2005/0003599) as applied to claim 19 and further in combination with Yu (U.S. 6,391,695).

Yeo further disclose the inducing layer having a lattice constant from .2 to about 2 percent larger than lattice constant of silicon due to layer being SiGe (Par. 0013), but does not appear to use of a double gate.

Yu (Fig 9) discloses double gate (14, 38).

It would have been obvious to form a double gate structure on the substrate of Yeo in order to increase density and high drive current as taught by Yu (Col. 2, Lines 7-8, 50-52).

Response to Arguments

Applicant's arguments filed December 13, 2006 have been fully considered but they are not persuasive based on the ineffective 1.131 declaration as explained above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Note, newly cited prior art discloses even prior to February 7, 2002 attaching a SiGe and silicon multilayer to an insulator layer on a substrate and then removing SiGe, see e.g. Kub et al. (U.S. 6,323,108).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ex. Mitchell, J.D.
March 4, 2007

CARL WHITEHEAD, JR.
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